Using the Agilent Technologies 16700 Series Logic Analysis System with the Xilinx ChipScope ILA

Product Note

This product note describes the ability to combine internal and external logic analysis traces in a time-correlated display on an Agilent Technologies 16700 Series logic analysis system. Agilent Technologies provides logic analysis capability for externally accessible signals. The Xilinx ChipScope ILA (integrated logic analyzer) "probes" internal signals of a Field Programmable Gate Array (FPGA). Using the two tools together provides digital design engineers with a powerful system debug solution that enables them to spend less time verifying chip functionality. No longer are designers forced to use a simulator to examine the state of internal nodes and attempt to correlate those results to captured data on a logic analyzer.

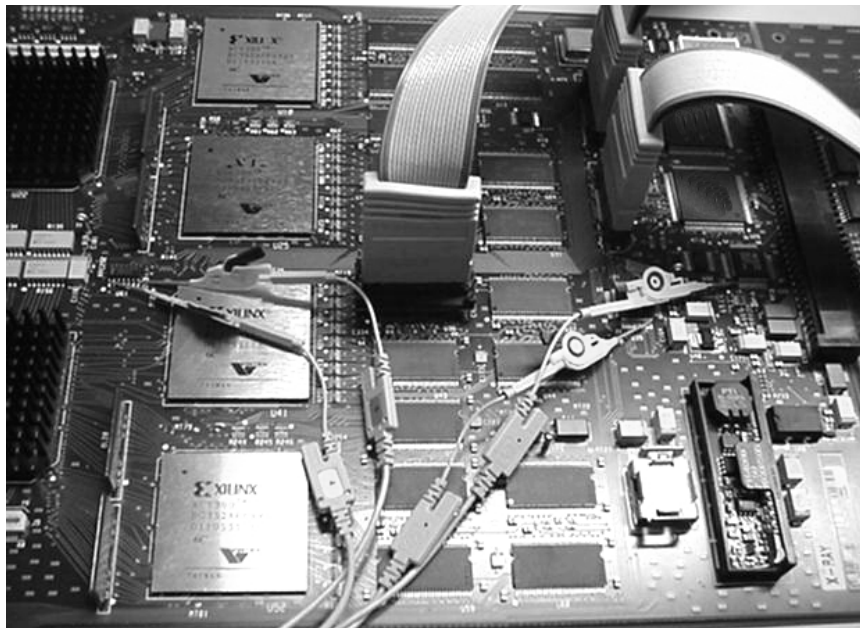| Agilent Technologies	Xilinx	Target System
16700 Series Mainframe	ChipScope ILA Software	Headers or test points
167xx Analyzer Module	Virtex, VirtexE or Spartan FPGA devices	JTAG port for MultiLinx cable
ILA Tool	Xilinx Internal Analyzer Modules	
	MultiLinx Cable	

Figure 1. Example of a circuit board with headers (upper right) and individual test points

Initial Setup Requirements

The user must have test points, headers or devices with packaging that can be probed on the circuit board. Figure 1 shows different methods of probing a circuit board. For probing information, refer to publication "*Probing Solutions for Agilent Logic Analysis Systems,*" 5968-4632E. The key here is that debugging capability requires access to the signals of interest. Once the ability to physically probe the target system exists, the user can use a 16700 Series logic analysis system to capture and analyze data. You will need the ILA correlation software tool installed on the 16700. This tool is available with version A.02.10.00 or higher.

You also need Xilinx (Virtex, VirtexE or Spartan II) devices to use the Xilinx ChipScope ILA. Figure 1 shows a board with Xilinx Virtex devices installed. You will need two free pins on the FPGA package that can be probed for trigger-in and trigger-out functions.

The Xilinx ChipScope ILA provides a means to probe signals internal to the Virtex families of FPGA devices. This

ILA can be configured to receive a trigger from an external source and drive a signal to trigger external equipment. We will use this capability along with the "Port In" and "Port Out" functions of the 16700 Series logic analysis system to perform correlated measurements with both Xilinx and Agilent logic analyzers.

Agilent Technologies

Take a Measurement with the ILA Triggered From an External Analyzer

We are going to use a simple 32-bit binary counter to demonstrate the ease of setting up and taking a measurement using both the Agilent Technologies and Xilinx logic analyzers. The counter is probed internally using the Xilinx ChipScope ILA and externally with an Agilent 16752A analysis module installed in a 16700 Series mainframe. We generated a 34-bit analyzer using the tools on the Xilinx website at www.xilinx.com to directly probe the counter registers. We will probe the same counter at the chip I/O using an Agilent 16752A logic analysis module in state mode. The basic system setup used for this example and any other type of combined measurement is shown in Figure 2. This diagram indicates the type of connections necessary between the different equipment to achieve a correlated display.
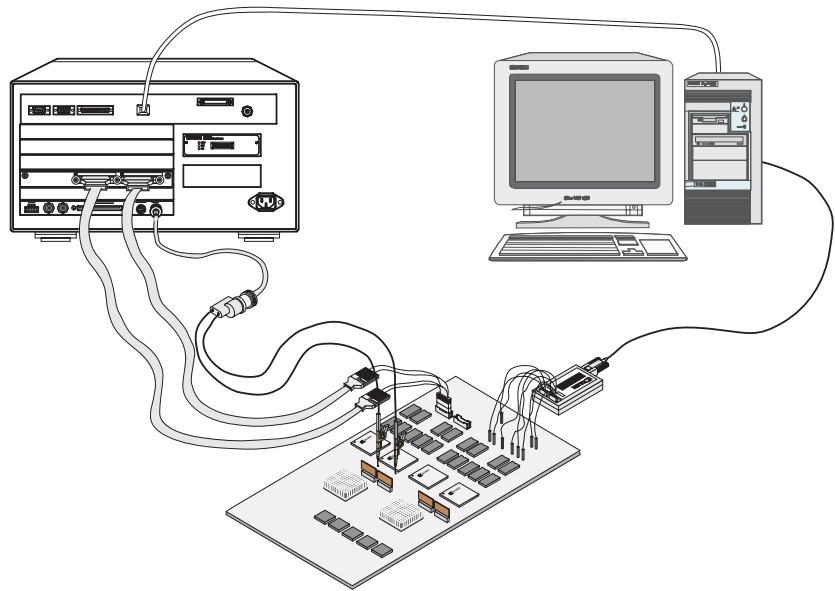

Figure 2. System connection diagram using an Agilent 16700 Series logic analysis system (left) and a Xilinx ChipScope ILA (right)

Setting up the Agilent Technologies 16700 Series Logic Analysis System

We will set up an Agilent 16700 to drive its external port out when the trigger condition is met. We do this from the main system window. Select the "Port Out" button to bring up its setup window (Figure 3). The port will be unselected and will not drive after system startup. We are selecting the analyzer in slot A as the arming analyzer for this example. You could use any of the Agilent logic analysis modules plugged into a 16700 Series mainframe for this purpose. We enable the port as "Pulsed" so that the output is only high for awhile after trigger, but not prior to trigger.
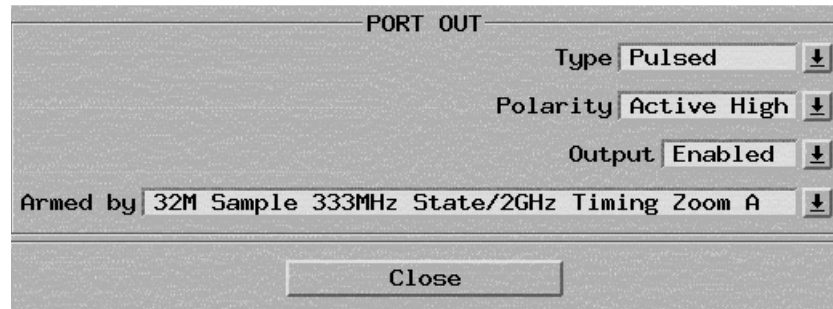

Figure 3. Desired output port settings

Once this setup is complete, you can configure the probing and trigger sequence as desired.

Our example is a state mode measurement. The clock for the state measurement must be the same clock that is used for the ILA measurement. The 16700 Series setup screen should look similar to Figure 4. We have combined two logic analyzer pods to create a 32-bit label named "Count". An additional signal named "agilent_corr_ref" is connected to the "Clock" input of pod A2 (see Figure 5) and is used as a data input to the 16700 Series system. This is the trigger out signal from the FPGA and is used to align the data sets generated by the ILA and the 16752A. We will discuss this signal later in this product note.
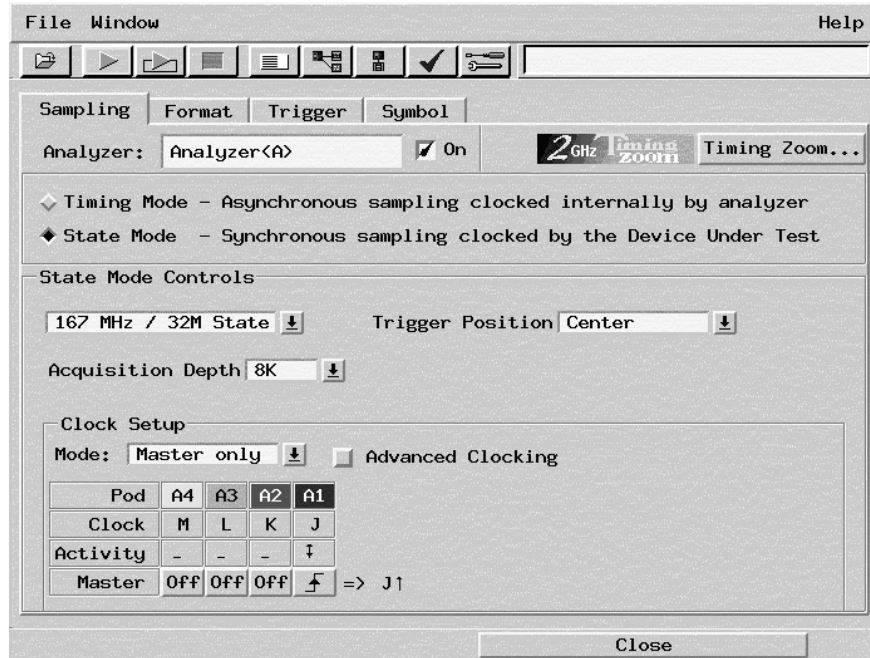

Figure 4. Setup for state measurement with 8 K samples. The clock is source from pod A1.

Note that the memory depth is user selectable, as is the actual clock setup. The memory depth is further determined by the model of logic analysis module installed in the 16700 Series mainframe. In this case we are using a 16752A module with a 32 M sample buffer, but we will use only 8 K of the available memory. We have connected the "Clock" probe of pod A1 to the FPGA input clock and are using it as our sample clock. This is the same clock used for the ILA.
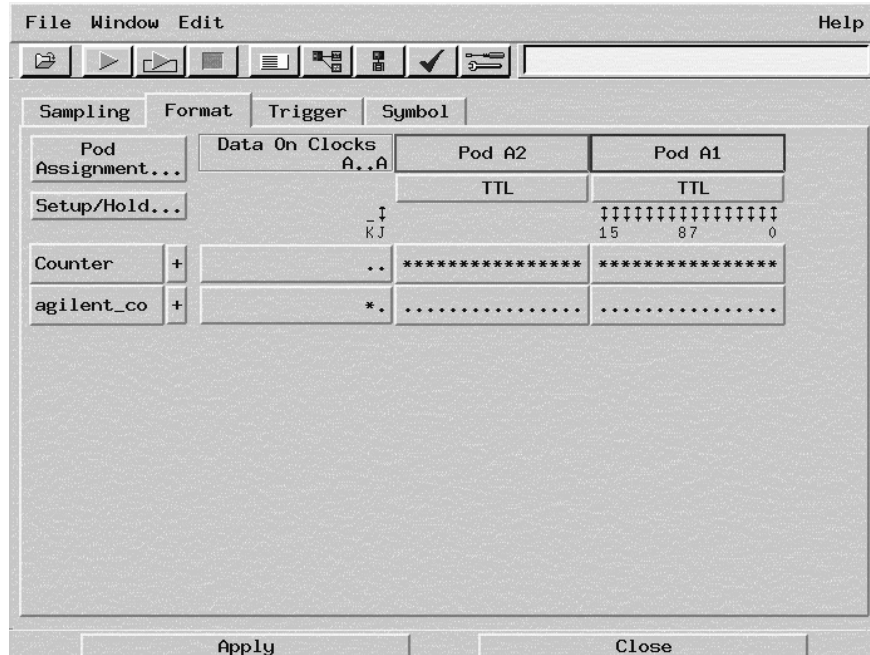

Figure 5. Pod setup using a 32-bit count and single bit for the synchronizing signal

The next step for the example is set-
ting up the trigger condition. We are
going to trigger on a count of '0' to
demonstrate the cross-triggering
capabilities of a 16700 Series logic
analysis system and an ILA. Notice
that the trigger action includes "arm
out" along with trigger and fill memo-
ry. The arm out action only appears
when the output port from the ana-
lyzer is used. Don't start the acquisi-
tion yet. We still need to set up the
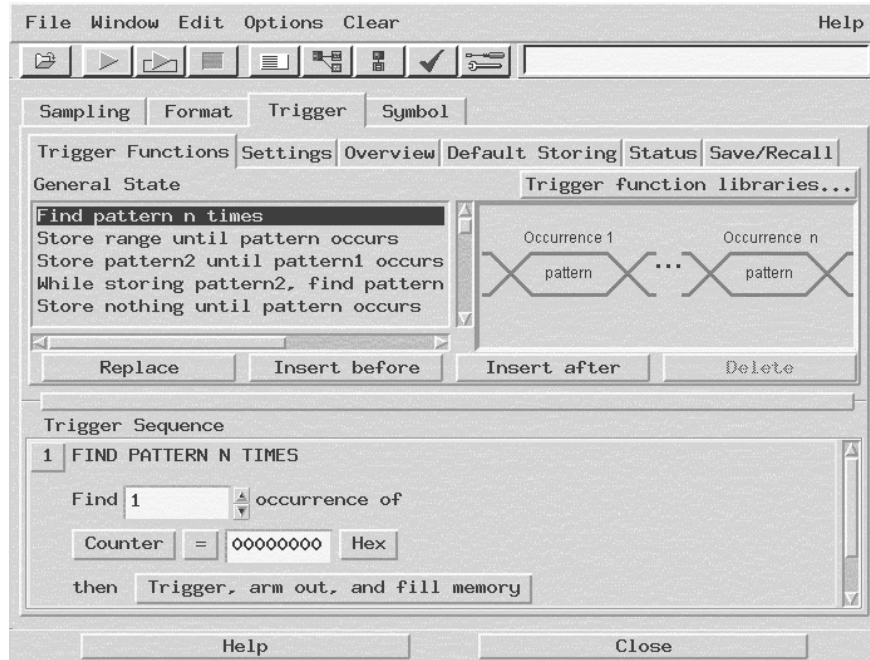ILA through the ChipScope interface.

Figure 6. Triggering on count of '0' with "arm out" active

Setting up the Xilinx ILA

We can directly probe internal signals
with the ILA. In this example, the
lower 32 bits of the ILA are probing
the counter registers. The 33rd bit is
probing the 15th bit of the control
bus. This signal is the internal repre-
sentation of the trigger out from the
ILA. A segment from the Verilog
source code for the example circuit is
listed below in Figure 7.

```
module top_apps (clk,led,count);
input clk;
output led;
output [31:0] count;
wire [41:0] control_bus0;
wire [31:0] count;

demo counter (
            .clk(clk),
            .led(led),
            .count(count));

ila_dd1024_dw33_tw32_e2 U0_ila_dd1024_dw33_tw32_e2 (
            .CONTROL(control_bus0),
            .CLK(clk),
            .DATA({control_bus0[14],count}),
            .TRIG(count));

icon U_icon (
            .CONTROL0(control_bus0));

endmodule
```

Figure 7. Sample of Verilog source code for the example circuit

We bring up the ChipScope software and set up the trigger condition as "macro" with EXT as the source. In addition, the capture mode is set up as "One Shot" (default). We enable the "Ext. Out" signal for synchronization purposes (we are probing this signal with both analyzers). The ILA is now set up to trigger when its external trigger input goes high. Starting the ILA at this point will arm it and force it to wait for the 16700 Series system to trigger.

Figure 8 shows the trigger position at 128 (out of 256 samples). The user can set the trigger to any valid location. The example screen also drives the external trigger-out signal even though the unit is not triggering any other analyzers. This signal will be used to correlate the data sets from the Xilinx ILA and the Agilent logic analysis module.
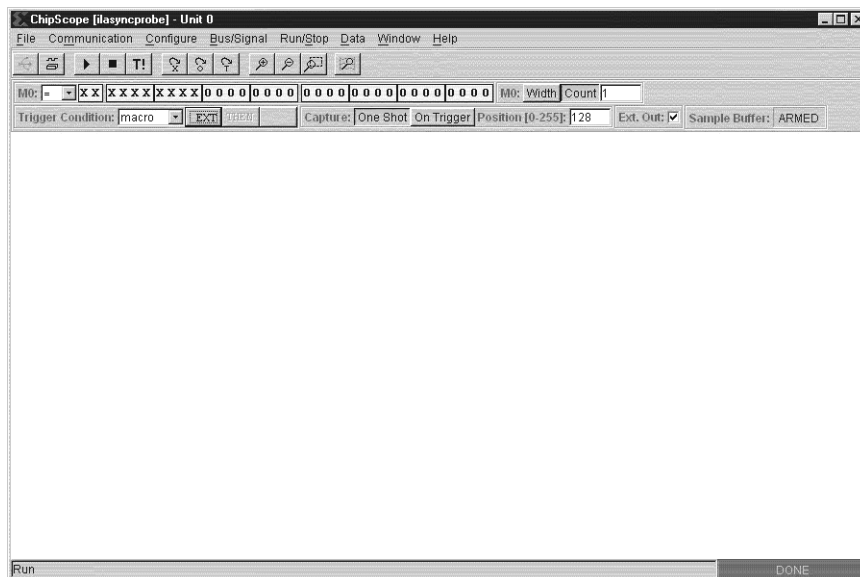

Figure 8. Xilinx ChipScope armed and ready for external trigger

Take the Measurement

The Xilinx ILA can now be started from the ChipScope interface. It will arm and wait for the trigger from the Agilent analysis module. The Agilent 16700 Series can then be started. Once its trigger condition is detected, both the Xilinx ILA and Agilent 16700 Series system will finish and display data. Figures 9 and 10 show both analyzers having completed an acquisition.
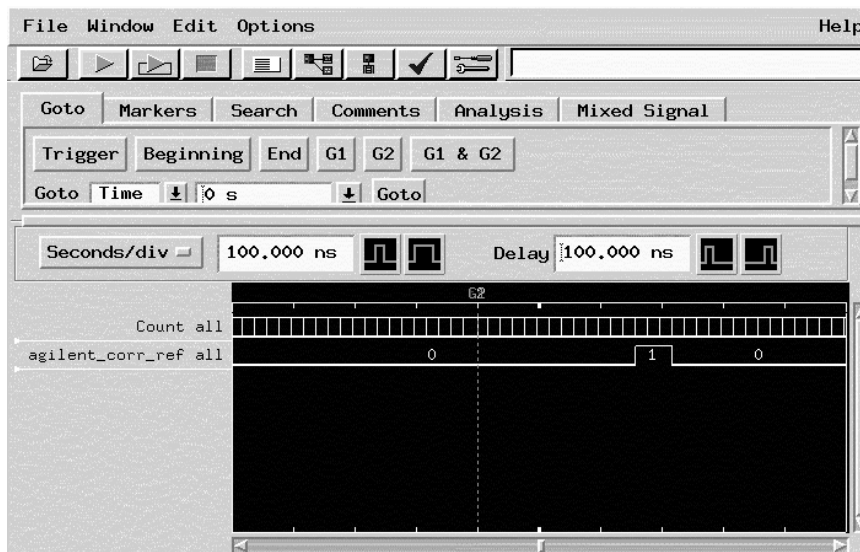

Figure 9. Agilent 16700 Series logic analysis system complete measurement

Reference Signal for Data Alignment

Aligning seemingly unrelated data sets can be difficult. The operation of trigger out and trigger in is dependent on the trigger mode of the Xilinx ILA (extended or basic). There is also a latency from the Agilent analysis module trigger and the output port signal. A simple solution is to find a common data transition between the ILA and the 16752A data sets. The trigger out from the ILA is an ideal signal for this purpose.

This signal is controlled by the Xilinx ILA, and can be simultaneously probed by the 16700 Series system and the ILA. The trigger-out signal from the ILA might not be identifiable from the Verilog source code. The ILA and ICON modules are macros that are not compiled, but instead inserted during FPGA implementation. They are treated as black boxes by the synthesis tools.

If you are using an ICON module compiled for a single ILA, then control_bus[14] is the external trigger-out signal. Otherwise, you will need to probe the external trigger-out signal using the ILA functions in the FPGA editor.

We have named the external trigger out from the Xilinx analyzer "agilent_corr_ref" to identify this special signal when working with combined waveforms.
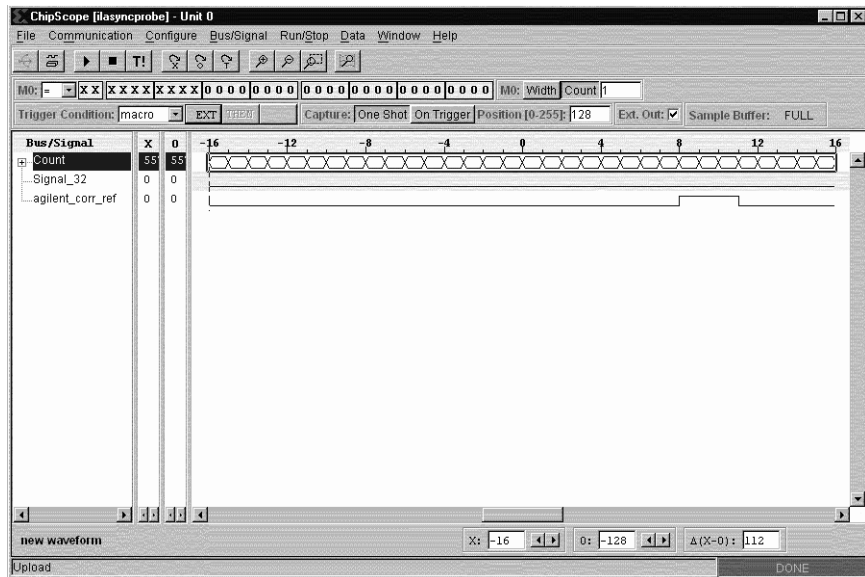

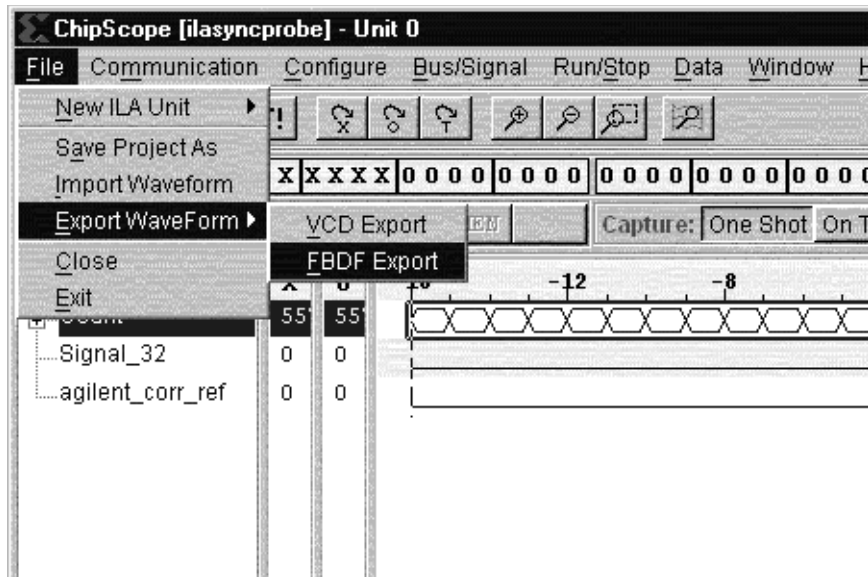**Figure 10. Xilinx ChipScope after complete measurement**

Figure 11. Export FBDF file from ChipScope

Export the ChipScope Data to FBDF

The interface between the Xilinx ChipScope and Agilent 16700 Series logic analysis system is through an Agilent Technologies Fast Binary Data Format (FBDF) file. The ChipScope tool can export its waveform directly to FBDF from the file menu.

The Agilent 16700 Series system can share a drive for Windows® use. This allows the user to directly export FBDF files to the Agilent 16700 Series system. If sharing is not possible, the file can be transferred to the 16700 Series system via FTP or a floppy disk.

Once the FBDF file is created and transferred to the Agilent 16700 Series, you use the file-in tool to read the file into a waveform or listing display through the ILA correlation tool. The result is a combined waveform or listing display that includes both data sets. The ILA correlation tool requires that the user enter the clock period, in nanoseconds, used for ILA data capture. This information is not available from the Xilinx FBDF file and must be entered manually. Double clicking on the ILA icon opens a window for the clock period entry (Figure 13). You also have the ability to select the name of the reference signal in this new window. The default name is "agilent_corr_ref". You can use any name as long as the name is the same in both data sets.
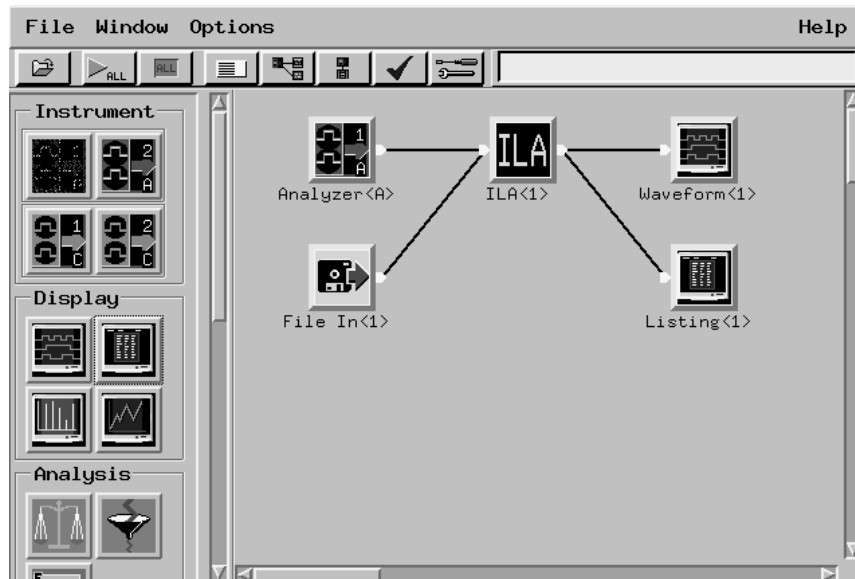

Figure 12. 16700 Series workspace showing ILA correlation tool. The "File In" tool is for the Xilinx ILA data
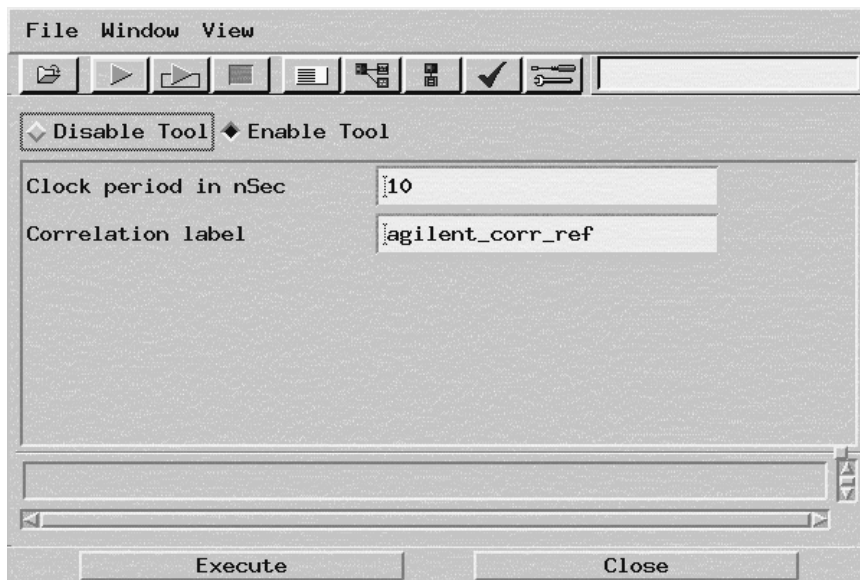

Figure 13. ILA tool setup window

The waveforms are automatically aligned using the reference signals in each data set. You can zoom in and out at this point and maintain the correct timing relationship of the data.
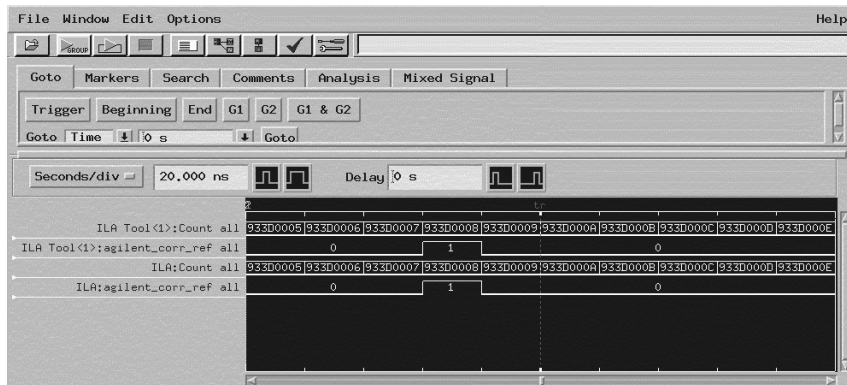

Figure 14. Waveform display showing correlated signals

Working with Trigger Generated from Xilinx ILA

The example in this product note demonstrates the ability to trigger the Xilinx ILA from the Agilent 16700 Series. Conversely, you can trigger the 16700 Series from the ILA. Both systems will still need to probe a common signal, which could be the trigger-out from the ILA. The auto data alignment will work with both types of trigger setups.

You will need to enable the Port In of the 16700 Series by using the Intermodule window to arm the desired logic analysis module from Port In. The module can then be set up to trigger on arm-in going true.

Figure 15. Setting up the 167xx analysis module to arm from Port In

How Do I Get the ILA Correlation Tool?

The ILA correlation tool used in this product note is available on the 16700 Series System Software CD-ROM, version A.02.10.00 or higher. The tool is located in the auxiliary-SW section. Follow the installation instruction provided with the CD-ROM.

Related Literature

Agilent Technologies 16700 Series Logic Analysis System product overview   5968-9961E

Probing Solutions for Agilent Logic Analysis Systems product overview   5968-4632E

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